

# Bus based parallel computers: A viable way for massive parallelism

A. Ferreira\* A. Goldman vel Lejbman\*\* S. W. Song\*\*\*

**Abstract.** In most distributed memory MIMD multiprocessors, processors are connected by a point-to-point interconnection network. Since interprocessor communication frequently constitutes serious bottlenecks, several architectures were proposed that enhance point-to-point topologies with the help of multiple bus systems so as to improve the communication efficiency. In this paper we study global communication on parallel architectures where the communication means are constituted *solely* by busses. We focus on the *hyperpath* and the *hypergrid* architectures, which are the bus-based versions of the well used point-to-point linear and grid interconnection networks. Using (hyper) graph theoretic concepts in order to model inter-processor communication in such networks, we developed a new tool called *simplification* in order to give extremely efficient algorithms for gossiping (all-to-all or total exchange communications).

## 1 Introduction

In most distributed memory MIMD multiprocessors, processors are connected by a point-to-point interconnection network. Since interprocessor communication frequently constitutes serious bottlenecks, several architectures were proposed to *enhance* point-to-point topologies with the help of multiple bus systems so as to improve the communication efficiency.

In this paper we study massively parallel systems where processors are connected by using *solely* by busses. These architectures can use the power of bus technologies, providing a way to interconnect much more processors in a simple and efficient manner. This represents a major issue in the construction of parallel computers, because a multiprocessor system with a large number (on the order of thousands) of processors cannot be provided with full connectivity and need

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\* CNRS - Laboratoire de l'Informatique du Parallélisme, École Normale Supérieure de Lyon, 46, Allée d'Italie, 69364 Lyon Cédex 07 - France. Partially supported by the PRC  $C^3$  and ANM of the French CNRS.

\*\* Department of Computer Science, Institute of Mathematics and Statistics, University of São Paulo, C.P. 20570 - São Paulo, SP 01498-970 - Brazil. Supported by FAPESP - Proc. No. 92/3991-0

\*\*\* Department of Computer Science, Institute of Mathematics and Statistics, University of São Paulo, C.P. 20570 - São Paulo, SP 01498-970 - Brazil. Supported by FAPESP - Proc. No. 93/0603-1 and CNPq - Proc. No. 306063/88-3 and PROTEM-CC/SP.

to operate by communication between processors. Furthermore, the multiple bus architecture has the desirable ability to expand. While a crossbar architecture needs a quadratic number of switches, a multiple bus system of  $P$  processors and  $B$  busses requires only  $BP$  switches, though with reduced connectivity. Without the underlying point-to-point network, such architectures are feasible and suitable for VLSI implementation, being able to interconnect a lot more processors, while keeping the diameter of the network small (see, for instance, [14] for a cell design incorporating a processor, its local memory and bus switches). For instance, 8100 processors can compose a 2-dimensional hypergrid – as defined in the next section –, where each processor is connected to at most four busses, each bus has 30 processors, and the distance between the farthest apart processors is as low as 10. Notice that this is better than a usual hypercube of the same size, and not as difficult to build, since it requires only 36 busses.

Common networks are usually modeled by a graph where processors are nodes and communication links are edges. On the other hand, bus interconnection networks (*BINs*, for short) are best modeled by a *hypergraph* [2], in which an edge is a subset of nodes. Each bus in the network is thus represented by an edge of the hypergraph [3, 13]. Several papers used derived models to propose and study new classes of interconnection networks for massively parallel computers. In [12], Scherson proposes the concept of “orthogonal graphs”, that can describe, for instance, binary  $m$ -cubes or meshes with busses in rows and columns. He also studies the routing problem in such architectures. Fiduccia [8] tackles the problem of pin optimality of interconnection networks, concluding that bused  $n$ -node hypercubes, where  $n$  busses run along the  $\log n$  dimensions of the hypercube, are pin-optimal. Hypergraphs are used by Szymanski [13] to model some photonic networks, where processors communicate through optical fibers carrying laser beams that have different wavelengths. Although little work has been done concerning algorithms in these new models, Bermond and Ergincan propose an excellent survey on structural problems related to *BINs* [4].

Another approach is to enhance existing point-to-point networks with multiple bus systems [1, 5, 10, 14], but this is out of the scope of this paper.

For deriving efficient communication patterns in *BINs* we developed a new tool called *simplification*. The idea is to construct a graph, to be called *representative graph*, from the original hyper-topology, in such a way that it will become easy to describe and perform communication schemes to the former that will fit to the latter, because the simplification concept also allows us to partially use some already known communication algorithms for usual networks.

By generalizing the notion of a linear network, we can design a *BIN* with the following features. Let  $\mathcal{P}_{n,m}$  be a parallel computer having  $nm$  processors,  $n - 1$  busses, with  $2m$  processors per bus, each processor being connected to at most two busses. In such an architecture, we show how to implement a gossiping (all-to-all) operation in at most  $m + n - 2$  steps. If we start from a 2- $d$  grid, our *BIN* will be denoted  $\mathcal{G}_2 = \mathcal{P}_{n_1,m_1}^1 \times \mathcal{P}_{n_2,m_2}^2$ . This is a parallel computer with  $n_1m_1n_2m_2$  processors,  $n_1n_2$  busses, each bus with  $2m_1$  or  $2m_2$  processors, where each processor is connected to at most four busses. We show that, in  $\mathcal{G}_2$ , we can